REMARKS

Claims 1-9 are pending in this application after this Amendment. Claims 1 is independent. In light of the remarks made herein, Applicants respectfully request reconsideration and withdrawal of the outstanding rejections.

In the outstanding Official Action, the Examiner rejects claims 1-3 and 9 under 35 U.S.C. §103(a) as being unpatentable over *Yiu et al.* (USP 5,859,649) in view of *Perlman* (USP 5,043,714); rejects claims 4 and 5 under 35 U.S.C. §103(a) as being unpatentable over *Yiu et al.* in view of *Perlman* and further in view of *Oh* (USP 5,901,274); rejects claim 6 under 35 U.S.C. §103(a) as being unpatentable over *Yiu et al.* in view of *Perlman* and further in view of *Eglit* (USP 5,850,207); and rejects claims 7 and 8 under 35 U.S.C. §103(a) as being unpatentable over *Yiu et al.* in view of *Perlman* and further in view of *Dye* (USP 5,706,478). Applicants respectfully traverse these rejections.

Claim Rejections – 35 U.S.C. §103(a) – *Yiu et al./Perlman*

In support of the Examiner's rejection of claim 1, the Examiner admits that *Yiu et al.* fails to teach or suggest data format and storage address information transfer to the display control section, wherein the display control section reads out the display data by specifying the address of the display data for one like which has a possibility to be displayed on the screen to the main memory from which the display data is transferred, based on the stored information, causing the data processing circuit to perform the data transfer and select the line memory to store the display data. The Examiner asserts that *Perlman* cures the deficiency of the teachings of *Yiu et al.* The Examiner asserts one skilled in the art would be motivated to combine the teachings of *Yiu et al.* because this provides for data storage in an efficient contiguously accessible memory location. Applicants respectfully disagree that there is motivation to combine the references as asserted by the Examiner and that the references teach all of the claim elements.

Yiu et al. discloses at col. 4, lines 4-21 as follows:

> FIG. 3 is a timing diagram of various signals of the data processing system of FIG. 1. Each clock cycle of clock signal SYSTEM CLOCK is labeled with a "t" followed by a number. Referring to both FIG. 2 and FIG. 3, LCD control module 28 uses both bus arbitration and data bursting to supply display data to line buffer 60 from system memory 30, as needed to refresh LCD screen 49. Line buffer 60 essentially comprises two or more line buffers and operate similarly to a first-in, first-out (FIFO) buffer. While display data is being pumped to LCD display 49 by display control block 61 from one of the line buffers of line buffer 61, the other line buffer can be updated from system memory 30. When line buffer 61 is empty, or almost empty, line buffer 60 asserts request data signal RD as a logic one to screen DMA 58. Screen DMA 58 fills line buffer 60 with display data from system memory 30 in bursts of a predetermined number of words. The predetermined number bursts can be either 8 or 16 in the illustrated embodiment.

One skilled in the art would appreciate that it is unnecessary and not advantageous to have contiguously accessible memory to provide video output to a display in the apparatus disclosed by *Yiu et al.* Video display data would be continuously updated row by row and refreshed on a frame by frame basis and, thus, does not have be contiguously accessible in memory.

In addition, the Examiner relies on cursor logic 62, frame rate control 64 and LCD interface 66 of Fig. 2 to teach the data processing circuit of claim 1. However, *Yiu et al.* discloses that these three components receives the output of line buffer 60. As such, *Yiu et al.* fails to teach or suggest a number of line memories, which store the display data converted by said data processing circuit per unit of the display line. As shown in Fig. 2, line buffer 60 stores data obtained from main memory. The output of line buffer 60 is then sent to cursor logic 62, frame rate control 64 and LCD interface 66.

For the reasons set forth above, Applicants respectfully submit that *Yiu et al.* nor *Perlman*, either alone or in combination, teach or suggest all of the claim elements. Further,

Applicants respectfully submit that there is no motivation to combine the references as asserted by the Examiner. As the Examiner has failed to provide references that teach or suggest all of the claim elements and further fails to provide sufficient motivation to combine the purported teachings of the references, Applicants respectfully submit that claim 1 is not obvious over the references as cited by the Examiner. It is respectfully requested that the outstanding rejection be withdrawn.

It is respectfully submitted that claims 2-9 are allowable for the reasons set forth above with regard to claim 1 at least based upon their dependency on claim 1.

Conclusion

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Catherine M. Voisinet (Reg. No. 52,327) at the telephone number of the undersigned below, to conduct an interview in an effort to expedite prosecution in connection with the present application.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Dated: June 19, 2006

Respectfully submitted,

By _____
Charles Gorenstein
Registration No.: 29,271
BIRCH, STEWART, KOLASCH & BIRCH, LLP
8110 Gatehouse Road
Suite 100 East
P.O. Box 747
Falls Church, Virginia 22040-0747
(703) 205-8000
Attorney for Applicant